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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

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Matrix display driver with energy recovery

The invention relates to an energy recovery matrix display driver circuit, and a matrix display apparatus with such a driver circuit.

Alternating voltages are required between electrodes of matrix displays like LCD's, Plasma Display Panels (PDP), Plasma Addressed Liquid Crystal displays (PALC), and Electro-Luminescent panels (EL). Due to a capacitance present between the electrodes, and required steep slopes of the alternating voltage, relatively large charge or discharge currents are required to reverse the polarity of the voltage across the capacitance. To minimize the power dissipation during the polarity reversion, driver circuits which comprise an energy recovery circuit in which an external inductance forms a resonance circuit with the capacitance are known from EP-A-0548051 and EP-A-0704834. Both these prior arts disclose an energy recovery circuit for a PDP.

A PDP may be driven in a sub-field mode wherein during a field or a frame of the video information to be displayed, a plurality of successive sub-fields or frames occur. A sub-field comprises an addressing phase and a sustaining phase. During the addressing phase, the plasma rows are usually selected one by one and data in conformance with the video information to be displayed is written into pixels of the selected row. During the sustaining phase, a number of sustain pulses is generated dependent on the weight of the sub-field. Pixels pre-charged during the addressing phase to produce light during the sustain phase will emit an amount of light during the sustaining phase which corresponds to the weight of the sub-field. The total amount of light produced by a pixel during the field or frame period of the video information depends on the one hand on weights of the sub-fields and on the other hand on during which ones of the sub-fields the pixel was pre-charged to produce light.

In a PDP, the electrodes may be the scan electrodes and the common electrodes. Cooperating scan electrodes and common electrodes form pairs which are each associated with one of the plasma channels. During the sustaining phase, the pairs of electrodes are driven with anti-phase square wave voltages generated by a so-called full-bridge circuit. The full-bridge circuit comprises a first series arrangement of a first and a

second controllable switch, and a second series arrangement of a third and a fourth controllable switch. A junction of main current paths of the first and the second switch is coupled to a scan electrode. A junction of main current paths of the third and the fourth switch are coupled to a common electrode. The first series arrangement and the second series arrangement being arranged in parallel across terminals of a power supply source. The main current path of the first switch is arranged between the scan electrode and a first one of the terminals, the main current path of the third switch is arranged between the common electrode and said first terminal. During a first phase of a sustaining period, two of the switches are open while two of the other switches are closed such that the power supply voltage supplied by the power supply source is available in a first polarity between the cooperating electrodes and thus across the capacitance. During a second phase of the sustaining period, the switches which were open during the first phase are closed now, and the switches which were closed are open now such that the power supply voltage supplied by the power supply source is available in the reversed polarity between the cooperating electrodes.

A detailed description of this prior-art circuit and its operation is given in the description of Fig. 1 and Fig. 2.

Although the prior-art energy recovery circuit provides an efficient energy recovery, this circuit produces a considerable amount of Electro-Magnetic Interference (EMI).

It is, inter alia, an object of the invention to provide an efficient energy recovery circuit which produces less Electro-Magnetic Interference.

To this end, a first aspect of the invention provides an energy recovery matrix display driver circuit as claimed in claim 1. A second aspect of the invention provides a matrix display apparatus comprising such an energy recovery matrix display driver circuit as claimed in claim 5. Advantageous embodiments are defined in the dependent claims.

At the end of a resonance period, when the current through the inductor changes polarity, this current has to follow a path that starts at one terminal of the inductor and ends at the other terminal of the inductor. In the prior-art, this current has to flow via several diodes and one of the full-bridge switches (which is referred to in the now following and in the claims as the second switch). Thus, this current will flow through a loop with a large area and consequently generate a large electromagnetic field. Further, as this second

switch has to withstand a large voltage, in a practical implementation, its impedance is quite high. Therefore, the voltage across the inductor will be quite high and thus an amount of energy stored in the inductor will be quite high. As the switch which connects the inductor and the capacitance to form a resonance circuit (this switch is referred to in the now following and in the claims as the first switch) has to be opened at or after the end of the resonant period to allow at a start of a next resonant period to change the polarity of the voltage across the capacitive load in the opposite direction with respect to the first resonance period, the energy stored in the inductor will cause a high frequent oscillation with a parasitic capacitance at the terminal of the inductor connected to the first switch.

The invention is based on the insight that this high frequent oscillation is a major contributor to the EMI produced. In practice, the problem of the prior art is even more severe as the current in the loop through the second switch has to flow through two or three diodes, causing across the inductor a voltage which is the addition of two or three diode forward voltages and the voltage across the second switch.

In the circuit in accordance with the invention, an extra switch circuit is connected in parallel with the inductor to keep the above mentioned current in an as small as possible loop. Further, the switch circuit has to withstand a lower voltage as the second switch and will have in a practical implementation a lower impedance. But most importantly, the two or three diodes are not within the loop. Even if a unidirectional switch circuit is required, only one instead of two or three diodes is in the loop. Thus in the circuit in accordance with the invention, the voltage across the inductor will be significantly lower than in the prior art. Consequently, the energy stored in the inductor is lower, and the EMI caused by the parasitic resonance will be significantly lower.

In an embodiment as claimed in claim 2, the switch circuit comprises a series arrangement of a diode and a controllable switch. This has the advantage over a controllable switch only that the timing of the on-time of the switch is less critical. It is no problem when the switch is on when the current through the inductor has a polarity such that the diode is blocking.

In an embodiment as claimed in claim 3, the energy recovery circuit as claimed in claim 2 has been made symmetrical to obtain an optimal efficiency in both resonance phases.

In an embodiment as claimed in claim 4, due to the presence of the switch circuit it is possible to close the second switch at a later instant to prevent current to flow

from the power supply voltage via the second switch to the capacitive load. In this way, less power is drawn from the power supply, and the efficiency even further improves.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawings:

Fig. 1 shows a detailed circuit diagram of a prior art matrix display driver circuit with energy recovery,

Fig. 2 shows waveforms of signals occurring in the circuit of Fig. 1,

Fig. 3 shows a detailed circuit diagram of an embodiment of a matrix display driver in accordance with the invention,

Fig. 4 shows waveforms of signals occurring in the circuit of Fig. 3, and

Fig. 5 shows a matrix display and a block diagram of circuits driving the matrix display.

Fig. 1 shows a detailed circuit diagram of a prior art matrix display driver circuit with energy recovery.

The driver circuit comprises a buffer capacitor CB arranged between a node Nb and ground. A series arrangement of an ideal switch S1 and a resistor R1 is connected between the node Nb and a node N1. A series arrangement of an ideal switch S4 and a resistor R4 is connected between the node Nb and a node N2. All series arrangements of an ideal switch and a corresponding resistor represent a practical switch (for example a MOS-FET) with an on-resistance equal to the resistor value. The resonance inductor L1 is arranged between a node Nj and a node Nc. The current IL1 through the inductor is defined to flow from the node Nj to the node Nc. The voltage VL1 across the inductor is the voltage difference between the node Nj and the node Nc. The node Nj is connected to the node N1 via a diode D1, and to the node N2 via a diode D6. The cathode of the diode D1 and the anode of the diode D6 are connected to the node Nj. A diode D13 has an anode connected to ground and a cathode connected to the node N1. A diode D11 has an anode connected to the node N2 and a cathode connected to a positive pole of a power supply source PS which supplies a power supply voltage Vcc. The other pole of the power supply source PS is connected to ground. A capacitor Cp is arranged in parallel with the power supply source PS. A series arrangement of an ideal switch S2, a resistor R2, and an optional diode D2 is

connected between the node Nc and the positive pole of the power supply source PS. The cathode of the diode D2 is directed to the node Nc. A series arrangement of an ideal switch S5, a resistor R5, and an optional diode D8 is connected between the node Nc and ground. The anode of the diode D8 is connected to the node Nc. Both the diodes D2 and D8 are not disclosed in the prior art. The capacitive load CL is connected between the node Nc and ground. The voltage across the capacitive load CL is denoted by Vc and is the voltage difference between the node Nc and ground. Vj denotes the voltage between the node Nj and ground. The current IR2 flows through the resister R2.

The essence of this circuit is to store the blind energy in a reservoir, which is the buffer capacitor CB, and to pass the energy back and forth to the load capacitance CL. This passing back-and-forth is realised by building two parallel-switched one-way current paths with opposing directions (S1 and D1, S4 and D6) and using a lossless inductor L1 in-between. The function of the inductor L1 is to ensure that the right amount of energy is passed to the load CL before stopping the current at reversal of current direction through the inductor. This occurs after a half period time of the resonance of the series resonance loop formed by the inductor L1 and the load capacitance CL. In order to operate efficiently, the buffer capacitor CB has a far greater value than the load capacitance CL, thus ensuring that the buffer voltage remains relatively stable regardless of charge transfer to and from the load CL. Hence the loop capacitance is approximately equal to the load CL. Assume that the total series resistance in the resonance loop is mainly formed by the switch resistance and parallel diode resistance and that the resonance loop has a resonance frequency fres. This means that the factor of blind energy retained after one cycle is:

$$e^{-\left(\frac{\pi R}{2\sqrt{\frac{L_1}{CL}}}\right)}$$

The switching time Tsw allowed is fixed by the time to gas breakdown. The Q in this loop is high and this means that the natural frequency is not shifted by damping, and thus:

$$f_{res} = \frac{1}{2\pi\sqrt{L_1 x CL}} = \frac{1}{T_{res}} \;\&\; T_{sw} = \frac{T_{res}}{2} \Rightarrow L_1 = \left(\frac{T_{sw}}{\pi}\right)^2 \frac{1}{CL}$$

It can be concluded that L1 and CL are inversely proportional in this circuit. Furthermore, by substituting the equation above for L, the amount of blind energy retained after one cycle can be written as:

$$e^{-\left(\frac{\pi^2 R * CL}{2Tsw}\right)}$$

Given the high quality factor Q of the resonance loop, the term 'R*CL' is small with respect to Tsw, and thus the above can be approximated by:

$$1-\left(\frac{\pi^2 RCL}{2Tsw}\right)$$

Hence, the blind energy lossfactor is approximately:

$$\left(\frac{\pi^2 RCL}{2Tsw}\right)$$

Inductor-switch can be placed in parallel without mutual interference. In this way, the load is spread across more circuits, or circuit resistance's are placed in parallel. Either way, the effect of placing n such circuits in parallel is to give the following approximate blind energy loss factor:

$$\left(\frac{\pi^2 RCL}{2nTsw}\right)$$

Based on the above, the following conclusions can be drawn:

1. An increased screen size gives an increased load CL and thus an equivalently increased loss factor.

2. An increased number of parallel circuits hyperbolically decrease the loss factor.

3. Faster gases for higher scanning frequencies, and more light from faster prime, etc., means a lower Tsw and thus equivalently increased loss factor.

4. A higher resolution and larger screen sizes (HDTV/SVGA) mean a lower Tsw and a higher capacitive load CL, respectively, and thus a quadratically increased loss factor.

For example, in a practical 21" plasma display the load CL was 28nF spread across 2 circuits. Tsw was set at 300 ns by using an inductor L1 of 0.7H in each circuit. The resistance per switch was in the order of 200 mOhms. The sustain cycle took about 9.6 us.

Fig. 2 shows waveforms of signals occurring in the circuit of Fig. 1. The horizontal axis represents the time t, the left hand vertical axis represents the current I in Amperes, and the right hand side vertical axis represents the voltage V. The values shown along the axis are merely intended as an example.

Assume that the circuit has been active long enough that the voltage Vb across the buffer capacitor CB has settled halfway between the supply and ground potential (i.e. Vb is Vcc/2). Assume the load CL is at ground potential with respect to the sustain side (the scan side of the load forms a virtual ground because it is switched to ground during the active phase of this circuit). All switches are open at start. The cycle begins when the switch S1 closes at the instant t1. Energy is then sent to the load CL from the buffer CB via the inductor L1 in a resonant way. When the switch S1 closes, the floating end of the inductor (the node Nj) is clamped to the buffer voltage Vb via the diode D1. Current then builds up through the inductor L1 until the load voltage Vc equals the buffer voltage Vb at the instant t2. After this, the voltage across the inductor L1 reverses and hence the current IL1 through it decreases. The switch 2, which is the switch through which the current for arcing is delivered after gas breakdown, is closed at just before the end of the energy recovery cycle (at the instant t3). At this point, the remaining energy is delivered to the load capacitance CL from the supply PS as well as from the buffer CB. The diode D2 is conducting. The inductor current IL1 reaches zero at the instant t4. If the diode D1 were ideal then at this point the current IL1 through the inductor L1 and the switch S1 would cease. However, diodes have a reverse recovery time and this means a small reverse current (energy from load CL to buffer CB) is able to build up in the inductor L1 before the diode D1 goes into reverse state. However, the current IL1 through the inductor L1 must be continuous when the diode D1 stops conducting, and thus the capacitance Cj at the node Nj charges up until the diodes D6 and D11 close due to

forward bias and the rest of the inductor current IL1 flows back to the inductor L1 through the supply PS and/or the capacitor Cp, and/or through the diode D2, depending on the impedances in both paths. The voltage VL1 across the inductor L1 is now approximately three diode drops (D6, D11, D2) plus the voltage drop across the resistance R2 of the switch S2. This means that the negative current through the inductor L1 decreases until the diodes D6 and D11 stop conducting (forward bias too low). The remaining energy in the inductor L1 then oscillates back-and-forth with the stray capacitance Cj at the node Nj, the average voltage at this node is equal to the load voltage Vc. In the situation the optional diode D2 is not present, the voltage across the inductor L1 will be approximately two diode drops plus the voltage drop across the switch S2.

A similar set of events occurs at the instant when the load voltage Vc is brought back to zero and the energy is returned to the buffer Cb. The switch S4 closes, the diode D6 conducts and the node Nj is clamped to the buffer voltage Vb. This gives rise to a reverse voltage across the inductor L1 and a current IL1 builds up from the load CL to the buffer CB through it. The switch 5 closes at the end of the resonance, helping to drain the charge out of the load CL. The current IL1 though the inductor L1 changes direction (goes positive). When the diode D6 stops conducting the capacitance Cj at the node Nj is discharged until the diodes D1 and D13 are forward biased. At this point, the inductor current IL1 flows through these diodes and D8. The reverse voltage across the inductor VL1 is now approximately three diode drops (D1, D13, D8) plus the voltage drop across the resistance R6 of the switch S5. This means that the positive current through the inductor L1 decreases until the diodes D1 and D13 stop conducting. The remaining energy in the inductor L1 then oscillates back-and-forth with the stray capacitance Cj at node Nj and the average voltage at this node Nj is equal to the load voltage Vc (i.e. ground potential).

Six primary areas of power loss in this circuit with respect to energy recovery are found to be important:

1. Circuit resistance including switches and diodes (see blind energy loss factor).
2. Diode forward drops during conduction in the branches of the switches S1 and S4.
3. Diode reverse recovery dissipation in the branches of the switches S1 and S4.
4. Energy built-up in the inductor L1 during diode reverse recovery.
5. Energy delivered to load CL directly from the supply PS via the switch S2 above and beyond replenishment.

6. Energy removed from the load CL directly to ground via the switch S5 above and beyond rest energy.

Fig. 3 shows a detailed circuit diagram of an embodiment of a matrix display driver in accordance with the invention. Same references in this Figure as in Fig. 1 denote the same components, signals, or nodes. The circuit of Fig. 3 differs from the circuit of Fig. 1 in that the diodes D11 and D13 have been deleted, and that a switch circuit has been added which is connected in parallel to the inductor L1. In the embodiment in accordance with the invention as shown in Fig. 3, the switch circuit comprises two series arrangements both arranged between the nodes Nj and Nc. The first series arrangement comprises a diode D3, an ideal switch S3 and a resistor R3. The diode D3 has a cathode directed towards the node Nc. The second series arrangement comprises a diode D9, an ideal switch S6 and a resistor R6. The diode D9 has a cathode directed towards the node Nj.

A control circuit CC supplies switching signals to control the switches S1 to S6.

Fig. 4 shows waveforms of signals occurring in the circuit of Fig. 3. The voltages shown in Fig. 4 are the same as the ones shown in Fig. 2 and are accordingly labeled the same.

Assume that the circuit of Fig. 3 has been active long enough that the buffer capacitor CB has settled halfway between the supply and ground potential (i.e. Vb = Vcc/2). Assume the load CL is at ground potential with respect to the sustain side (the scan side of the load CL forms a virtual ground because it is switched to ground during the active phase of this circuit). All active switches are open at start.

The cycle begins when switch S1 closes at the instant t1'. Energy is then sent to the load CL from the buffer CB. When the switch S1 closes, the floating end of the inductor L1 (node Nj) is clamped to the buffer voltage Vb via the diode D1. Current then builds up through the inductor L1 until the load voltage Vc equals the buffer voltage Vb at the instant t2'. After this, the voltage VL1 across the inductor L1 reverses and hence the current IL1 decreases. The switch S3 (enabling the flywheel diode D3 to conduct) is closed before the end of the energy recovery cycle anytime after the voltage across the inductor L1 reverses (from the instant t2' onwards to the instant t3'). The inductor current IL1 reaches zero at the instant t3'. If diodes were ideal then at this point the current IL1 through the inductor L1 and the switch S1 would cease. However, diodes have a reverse recovery time

and this means a small reverse current (energy from the load CL to the buffer CB) builds up in the inductor L1 before the diode D1 goes into reverse. However, the current IL1 through the inductor L1 must be continuous when the diode D1 stops conducting, and thus the capacitance Cj at the node Nj charges up until the flywheel diode 3 closes due to forward bias and the rest of the inductor current IL1 flows back to the inductor L1 through this diode D3. The voltage VL1 across the inductor L1 is now approximately plus one diode drop. This means that the negative current through the inductor L1 decreases. This voltage drop VL1 across the inductor L1 is far less than in the case of the prior-art circuit so that the rate of decrease of the current IL1 through the inductor L1 is lower than in the prior-art circuit. The remaining energy in the inductor L1 once the diode D3 stops conducting (which is far lower than in the first circuit) then oscillates back-and-forth with the stray capacitance Cj. The switch S2 (the switch through which the current for arcing is delivered after gas breakdown) is closed after the energy recovery cycle (at the instant t5'). At this point, the remaining energy is delivered to the load capacitance CL from the power supply PS.

A similar set of events occurs at the instant t6' when the load voltage Vc is brought back to zero and the energy is returned to the buffer Cb. The switch S4 closes, the diode D6 conducts and the node Nj is clamped to the buffer voltage Vb. This gives rise to a reverse voltage across the inductor L1, and a current builds up from the load CL to the buffer CB through it. The switch S6 closes, in this example, 150 to 300 ns later, activating the second flywheel diode D9. The current IL1 though the inductor L1 changes direction (goes positive). When the diode D6 stops conducting, the capacitance Cj at node Nj is discharged until the flywheel diode D9 is forward biased. At this point, the inductor current IL1 flows through this diode D9. The voltage VL1 across the inductor L1 is now approximately minus one diode drop. This means that the positive current through the inductor decreases until the diode D9 stop conducting. The small amount of energy in the inductor L1 then oscillates back-and-forth with the stray capacitance Cj, and the average voltage at the node Nj is equal to the load voltage VC (i.e. ground potential). The switch S5 closes, in this example 300 ns later, helping to drain the charge out of the load CL.

The embodiment of the invention shown in Fig.3 offers an improved EMI behaviour than the prior-art circuit due to the shorter current flow and the lower inductor residual energy.

The driver circuit in accordance with the invention offers some savings now but these will become more pronounced if cycle time is reduced and/or Schottky flywheel

diodes become applicable (at the moment the breakdown voltage is insufficient and the plasma voltages are too high).

The delay of the instant at which the switches S2 and S5 are closed until after the energy recovery branches have ceased to conduct (for example, the switches S2 and S5 are closed 400 ns after the switches S1 and S4, respectively), removes losses due to energy delivered to load CL directly from the supply PS via the switch S2 above and beyond replenishment, and due to energy removed from the load CL directly to ground via the switch S5 above and beyond rest energy, respectively. Although this switch-on delay improves the efficiency, it is not essential to the invention.

The energy built-up in the inductor L1 during diode reverse recovery may be reduced if the supply VB is decoupled with a capacitor. This effect is due to the fact that the inductor current IL1 is forced into charging the supply decoupling capacitor Cp, and this energy is reused later. On the other hand this same charge is drawn out of the load capacitor CL reducing its voltage Vc, which causes increased replenishment losses in the switch S5. Given that about 50% of the replenishment energy is lost, this means that the losses are more or less unchanged if supply decoupling is performed (otherwise they increase). The real problem with this approach is that, without the extra switch circuit connected in parallel with the inductor L1, if the same gas breakdown time exists, the value of the inductor L1 must be slightly less than before in order to end energy recovery before the switches S2 and S5 are switched on. This causes a poorer performance due to the circuit resistance including switches and diodes.

Fig. 5 shows a matrix display and a block diagram of circuits driving the matrix display. The matrix display shown is a PDP of the kind in which the n plasma channels PC1, ..., PCn extend in the horizontal direction, and the m data electrodes DE1, ..., DEm extend in the vertical direction. Intersections of the plasma channels PC1, ..., PCn and the data electrodes DE1, ..., DEm are associated with the pixels. A pair of cooperating select electrode SEi and common electrode CEi is associated with a corresponding one of the plasma channels PCi. A select driver SD supplies scan pulses to the n select electrodes SE1, ..., SEn. A common driver CD supplies common pulses to the n common electrodes CE1, ...,CEn. A data driver DD receives a video signal Vs and supplies m data signals to the m data electrodes DE1, ..., DEm. A timing circuit TC receives synchronization signals S belonging to the video signal Vs to supplies control signals Co1, Co2, and Co3 to the data

driver DD, the select driver SD, and the common driver CD to control the timing of the pulses and signals supplied by these drivers.

During the addressing phase of the PDP, the plasma channels PC1, ..., PCn usually are ignited one by one. An ignited plasma channel PCi has a low impedance. The data voltages on the data electrodes determine an amount of charge in each of the plasma volumes (the pixels) associated with the data electrodes and the low impedant plasma channel PCi. A pixel preconditioned by this charge to produce light during the sustain period succeeding the addressing period will lit during this sustain period. A plasma channel PCi which has a low impedance is further referred to as a selected line (of pixels). During the addressing phase, the data signals to be stored in the pixels of a selected line are supplied line by line by the data driver DD. During the sustaining phase, the select driver and the common driver supply select pulses and common pulses, respectively to all the lines in which data has been stored during the preceding addressing phase. The pixels precharged to lit will produce light each time the associated plasma volumes are ignited. A plasma volume will be ignited when it is precharged to do so and the sustain voltage supplied across the plasma volume by the associated select electrode and common electrode changes a sufficient amount. The number of ignitions determine the total amount of light produced by the pixel. In a practical implementation, the sustain voltage comprises pulses of alternating polarity. The voltage difference between the positive and the negative pulses is selected to ignite plasma volumes precharged to produce light, and to not ignite the plasma volumes precharged to not produce light.

The invention is particularly useful during the sustain period wherein many plasma volumes will be ignited at the same time. All these plasma volumes form a large capacitance between the select electrodes and the common electrodes. In practice this capacitance is even larger because these electrodes have a capacitive coupling with other parts of the flat panel display. In this situation, the capacitance CL is formed by the capacitance mentioned in the previous sentence. The capacitance CL may be constituted by pixels of one or a group of the select electrodes. The switches S1 to S6 are part of either the select driver SD or the common driver CD.

Although Fig. 5 shows a special PDP, the invention is relevant to other PDP's. For example, the plasma channels may extend in the vertical direction, adjacent plasma channels may have an electrode in common. Or more general, the invention is relevant to all flat panel displays wherein a voltage over a capacitance has to change polarity regularly, such as PDP's, LCD's, or EL displays.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims.

The circuit is described with respect to the sustain function in a Plasma display panel (PDP). The circuit can be adapted for use in column and scan circuits in a PDP, and as anode switch and ramp-generator functions in Plasma Addressed Liquid crystal displays, and as the drive circuit for LCD's.

In the Figures, the load capacitance CL is connected to ground. In practice, for example for a Plasma Display Panel, the load capacitance CL may be connected between the scan and sustain electrodes as usual. Both ends of the load capacitor CL than receive pulses.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of other elements or steps than those listed in a claim. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware.

CLAIMS:

1. An energy recovery matrix display driver circuit for generating a voltage (Vc) having a periodically changing polarity across a capacitive load (CL), said driver circuit comprising:

an inductor (L1) being coupled to the capacitive load (CL),

a first switch (S1) for creating, during a resonance period (Tr), a resonance circuit including the inductor (L1) and the capacitive load (CL) to change said voltage (Vc) from a first polarity to a second polarity, and a second switch (S2) for coupling, after the resonance period, the capacitive load (CL) to a power supply voltage (Vcc) having the second polarity,

a switch circuit (S3, D3, S6, D9) connected in parallel with the inductor (L1) for circulating a current (IL1) through the inductor (L1) in a loop formed by said switch circuit and said inductor (L1), said loop being closed not later than an instant at which said current (IL1) changes polarity at the end of the resonant period (Tr), and

a control circuit (CC) for controlling the first switch (S1), the second switch (S2), and the switch circuit to periodically open and close.

2. An energy recovery matrix display driver circuit as claimed in claim 1, characterized in that the switch circuit comprises a series arrangement of a diode (D3) and a controlled switch (S3), said series arrangement being connected in parallel with the inductor (L1), said controlled switch (S3) being closed not later than the instant at which said current (IL1) changes polarity at the end of the resonant period (Tr), said diode (D3) being poled to conduct said current (IL1) after it changed polarity.

3. An energy recovery matrix display driver circuit as claimed in claim 2, characterized in that the switch circuit further comprises a series arrangement of a further diode (D9) and a further controlled switch (S6), said further series arrangement being connected in parallel with the inductor (L1), said further controlled switch (S6) being closed not later than an instant at which said current (IL1)changes polarity at the end of a further resonant period (Tr') in which the voltage across the capacitive load (CL) changes polarity in

an opposite direction with respect to the first mentioned resonant period (Tr), said further diode (D9) being oppositely poled with respect to the first mentioned diode (D3).

4. An energy recovery matrix display driver circuit as claimed in claim 1, characterized in that the control circuit (CC) is adapted to close the second switch (S2) after the instant at which said loop is closed.

5. A matrix display apparatus comprising a matrix display panel with a matrix of pixels associated with intersecting electrodes, an energy recovery matrix display driver circuit for generating a voltage (Vc) having a periodically changing polarity across a capacitive load (CL), said driver circuit comprising:

an inductor (L) being coupled to the capacitive load (CL),

a first switch (S1) for creating, during a resonance period (Tr), a resonance circuit including the inductor (L1) and the capacitive load (CL) to change said voltage (Vc) from a first polarity to a second polarity, and a second switch (S2) for coupling, after the resonance period (Tr), the capacitive load (CL) to a power supply voltage (Vcc) having the second polarity,

a switch circuit (S3, D3, S6, D9) connected in parallel with the inductor (L1) for circulating a current (IL1) through the inductor (L1) in a loop formed by said switch circuit and said inductor (L1), said loop being closed not later than an instant at which said current (IL1) changes polarity at the end of the resonant period (Tr), and

a control circuit (CC) for controlling the first switch (S1), the second switch (S2), and the switch circuit to periodically open and close.

ABSTRACT:

In the matrix display driver circuit with an energy recovery inductor (L1), a switch circuit (S3, D3, S6, D9) is connected in parallel with the inductance (L1) to keep the inductor current (IL1) in an as small as possible loop, and to keep the voltage (VL1) across the inductor (L1) as low as possible. Consequently, the energy stored in the inductor is lower, and the EMI caused by the parasitic resonance of the inductor (L1) with parasitic capacitances Cj will be significantly lower.

(Fig. 3)

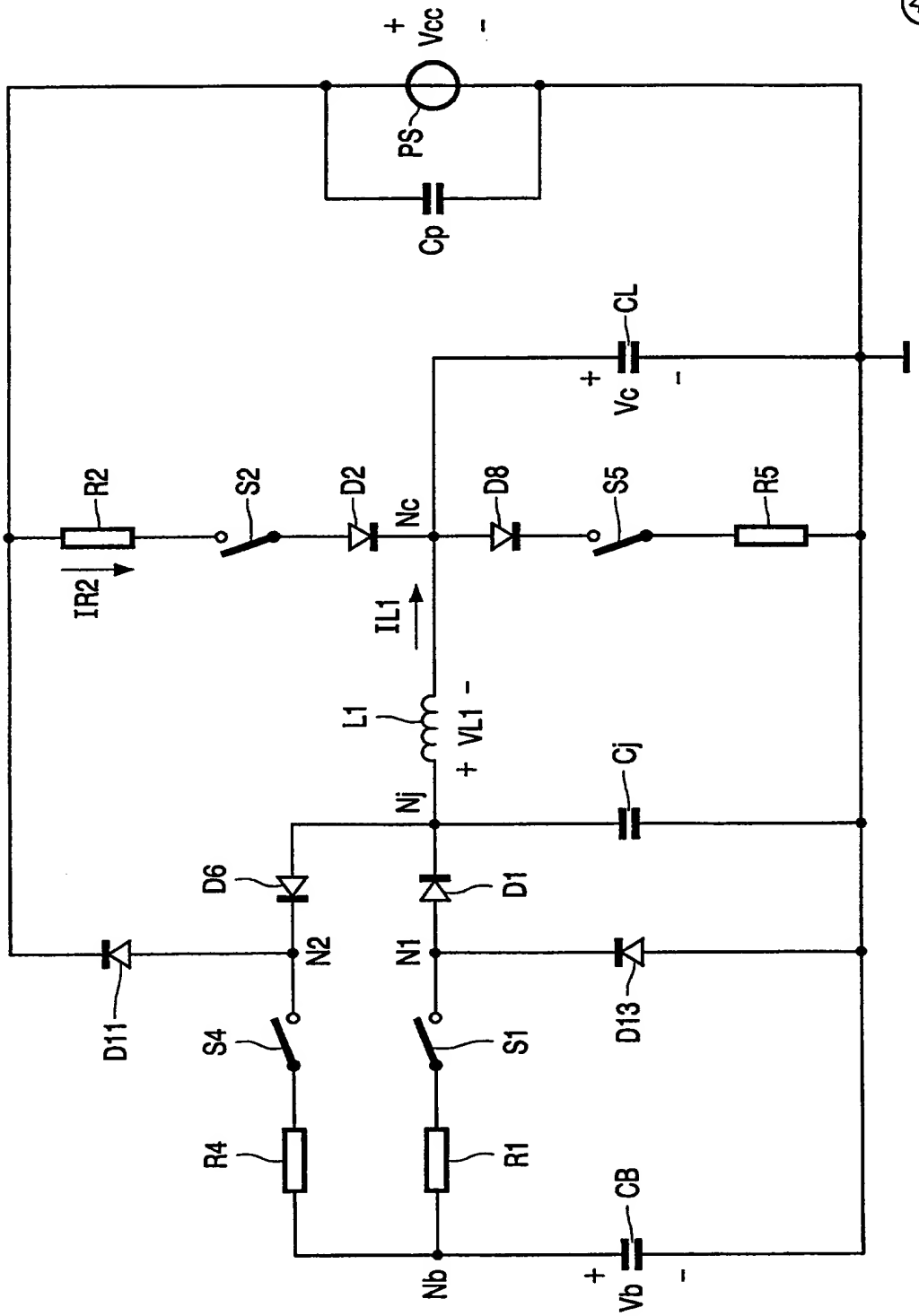

FIG. 1

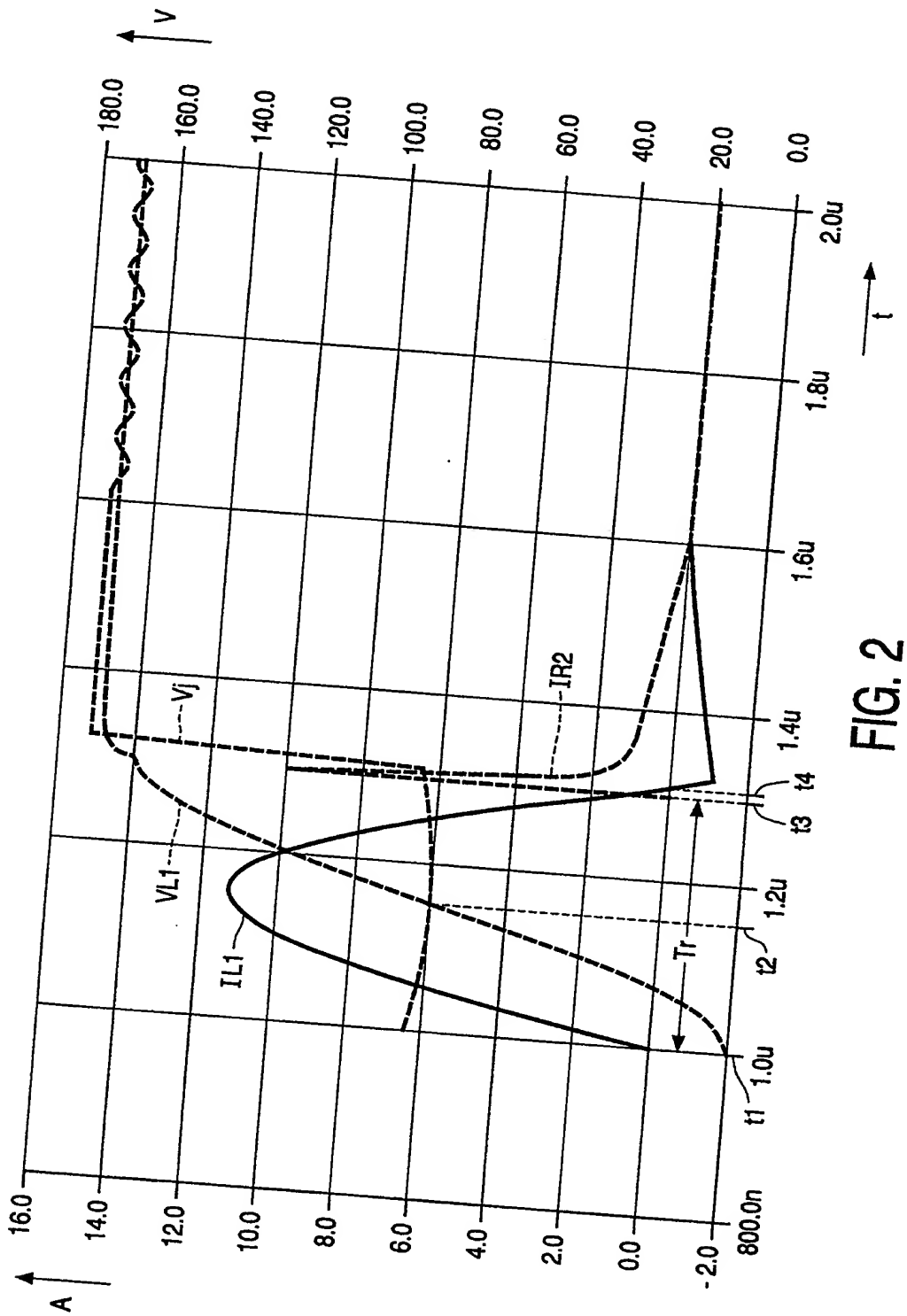
V
180.0
160.0
140.0
120.0
100.0
80.0
60.0
40.0
20.0
0.0
2.0u
1.8u
1.6u
1.4u
1.2u
1.0u
800.0n
t
A
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
Vj
VL1
IL1
TR2
Tr
t1
t2
t3
t4

FIG. 2

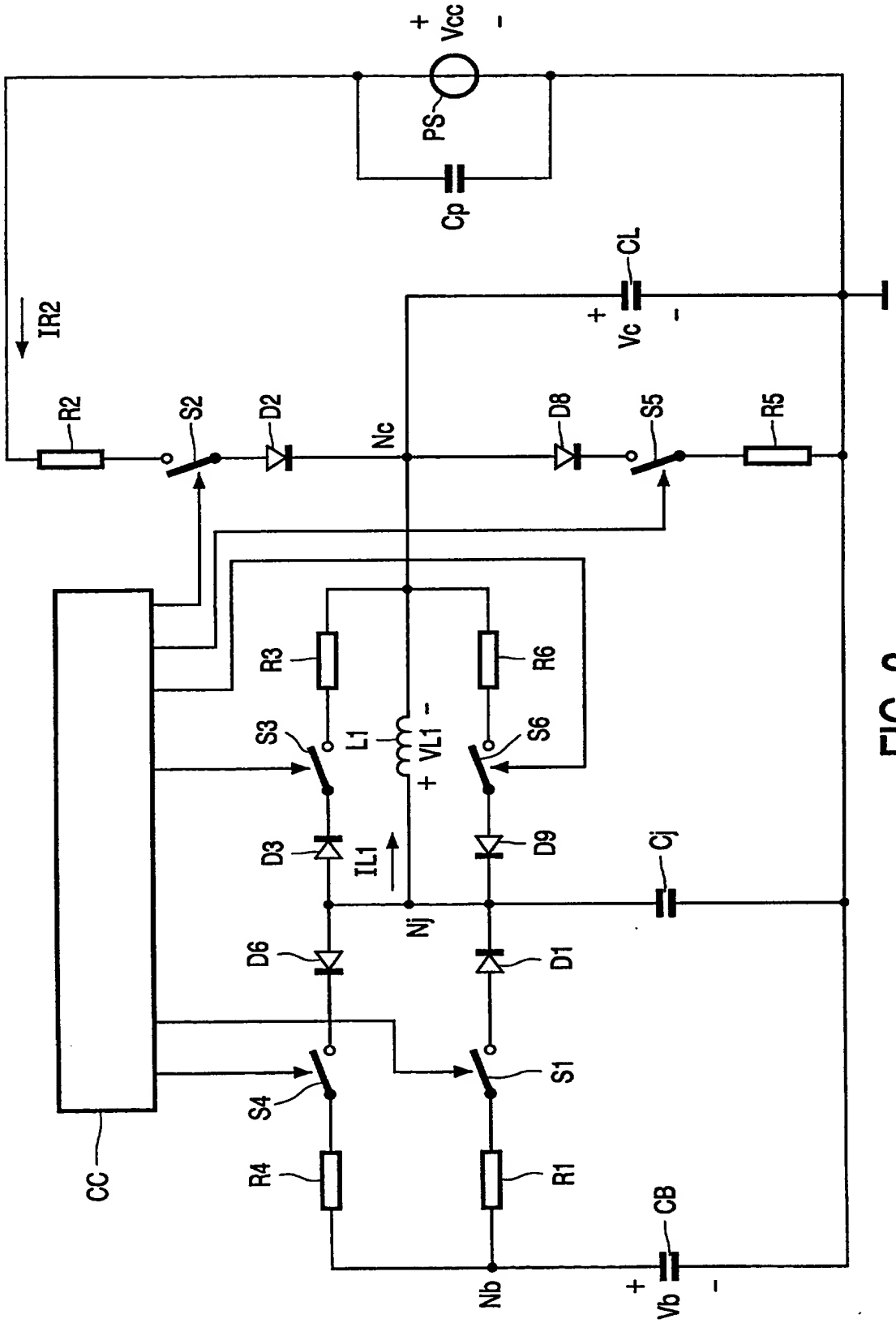
+ Vcc -
PS
Cp
CL
+ Vc -
IR2
R2
S2
D2
Nc
D8
S5
R5
R3
R6
S3
L1
+ VL1 -
S6
D3
IL1
D9
Cj
Nj
D6
D1
S4
S1
CC
R4
R1
CB
Nb
+ Vb -

FIG. 3

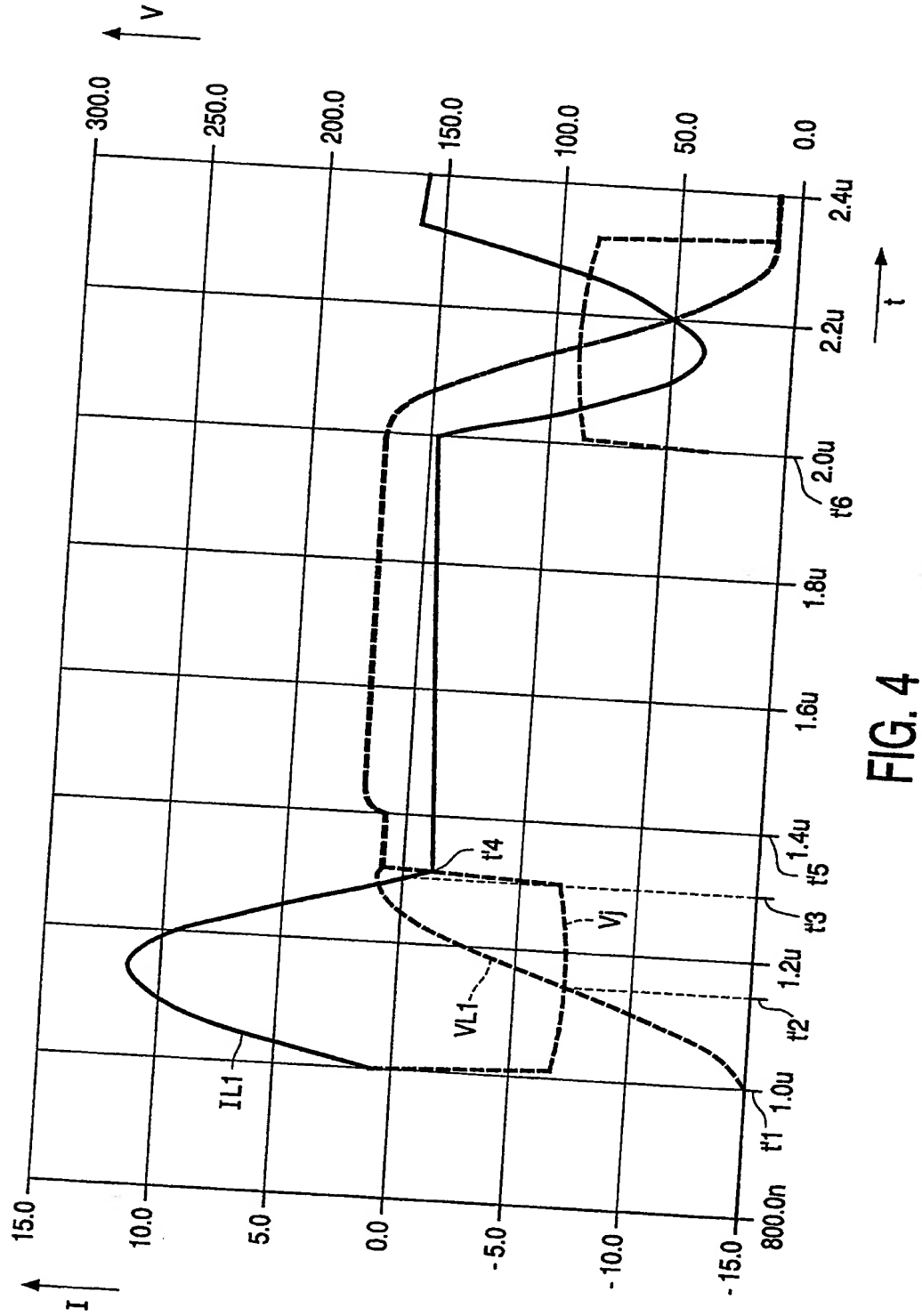
V
300.0
250.0
200.0
150.0
100.0
50.0
0.0
2.4u
2.2u
t
2.0u
t'6
1.8u
1.6u
1.4u
t'5
t'4
t'3
Vj
1.2u
t'2
VL1
IL1
1.0u
t'1
800.0n
I
15.0
10.0
5.0
0.0
-5.0
-10.0
-15.0

FIG. 4

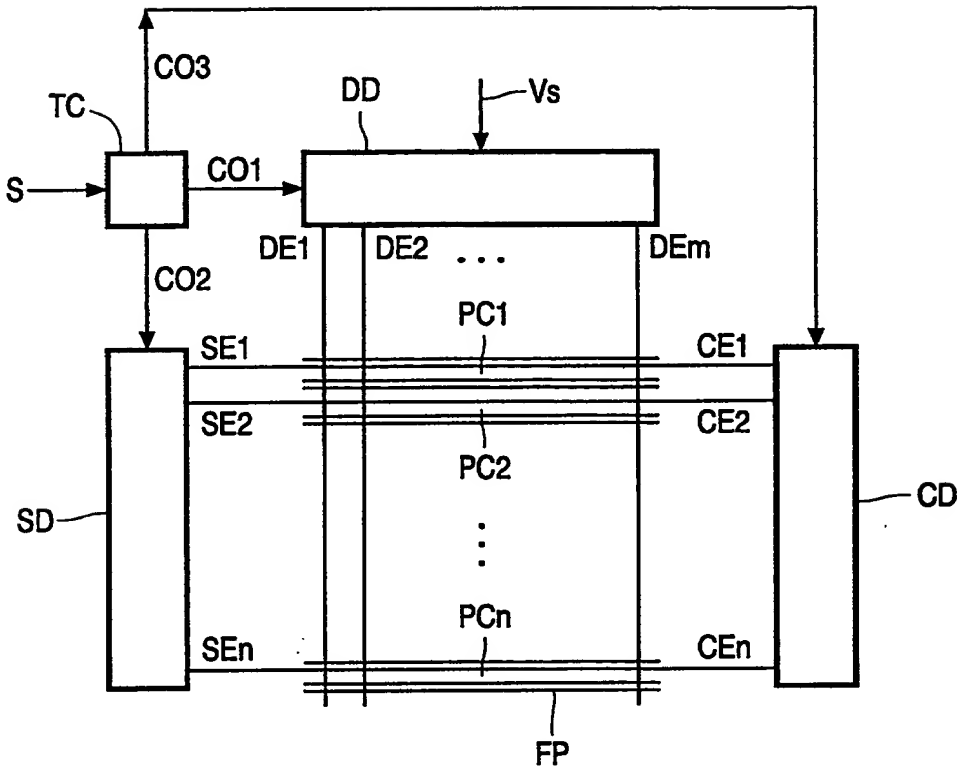
CO3
TC
DD
Vs
S
CO1
DE1
DE2
DEm
CO2
PC1
SE1
CE1
SE2
CE2
PC2
SD
CD
PCn
SEn
CEn
FP

FIG. 5